IMAGE SENSING STRUCTURE

Field of the Invention

[0001] The present invention relates to an image sensing structure, and in particular but not exclusively, to an image sensing structure comprising a photodiode that provides highly accurate matching between pixels.

Background of the Invention

[0002] Due to tolerances in the manufacturing process of photodiodes used in solid state imaging devices, there is usually a mismatch in sensitivity between pixels. In the case of a camera that takes pictures to be viewed by humans, the tolerances can be relatively low while creating an image of acceptable accuracy. A mismatch of around five percent is acceptable. However, for other applications such as cameras used for machine vision or optical mice, the allowable mismatch is much less, typically around one percent.

[0003] One way of improving such a mismatch is to remove it at the system level using calibration and compensation techniques. However, calibration requires special setup and also storage of the compensation coefficients. Compensation requires real-time processing, while costing silicon and consuming power. Hence, both

these techniques are complex to perform and are expensive.

[0004] The areas of technology requiring an improvement in such a mismatch are the areas that are commercially expanding. Therefore, there is a need for a photodiode structure that provides improved matching between pixels.

Summary of the Invention

[0005] According to the present invention there is provided a photodiode as claimed in the attached claims.

Brief Description of the Drawings

[0006] The present invention shall now be described, by way of example only, with reference to the accompanying drawings, in which:

[0007] FIG. 1 shows a first prior art image sensing structure;

[0008] FIG. 2 shows a second prior art image sensing structure;

[0009] FIG. 3 shows an image sensing structure in accordance with a first embodiment of the present invention;

[0010] FIG. 4 shows an image sensing structure in accordance with a second embodiment of the present invention; and

[0011] FIG. 5 shows an image sensing structure in accordance with a third embodiment of the present invention.

Detailed Description of the Preferred Embodiments

[0012] In transistor fabrication, multiple transistors of similar conductivity types are commonly located in a single well. In normal use, the well is reverse biased with respect to the transistor and the substrate, and there is virtually no current flowing into or out of the well and transistor. The transistors therefore do not interact, and so the electrical properties of the well are usually ignored.

[0013] However, the situation with photodetectors is very different. Incident light creates a current that flows into and/or out of the well, and the well's capacitance often determines the photodetector's sensitivity. Thus, the electrical properties of the well are very important to the operation of the detector. In a CMOS image sensing structure, the voltage out is governed by the equation: Voltage out = (number of photons x quantum efficiency x time x electronic charge)/capacitance of the sense node).

[0014] As the light collection (number of photons), conversion (quantum efficiency) and collection process is largely the same for all pixels, the variation in the capacitance of the sense node is the main cause of variations in sensitivity. These variations are due to manufacturing tolerances, and are fixed for a particular sensor, giving the name fixed pattern noise (FPN). Since the variation is fixed and not random, it is more accurately called photo response non-uniformity (PRNU).

[0015] FIG. 1 shows a common form of a CMOS image sensing structure. An epitaxial layer 10 is formed on a P-type substrate 12. A photodiode comprising an N-well collection node 14 with surrounding P-wells 16 is

formed in the epitaxial layer 10. The collection node 14 has a conductor 18 attached which carries a signal to a transistor 20, which is part of the corresponding readout electronics.

[0016] The photodiode illustrated in FIG. 1 is a relatively small photodiode, having a width of less than 10 μm. Typically, such a photodiode will have a width of between 4 and 6 μm. As also illustrated in FIG. 1, the epitaxial layer 10 has a depth between 4 and 5 μm, and both the N-well and P-wells have a depth of 3 μm, as measured from the upper surface of the epitaxial layer 10.

[0017] Light 22 impinging on the semiconductor produces electron/hole pairs. There is an electron field around the sense node 14 to attract the electrons there. This electron field is a combination of doping and applied voltage. The position at which electrons e1-e4 are freed from the silicon atoms is a statistical process, but is wavelength dependent. For visible light (typical wavelengths from 450 to 650 nm) impinging on silicon, the greatest production of electrons occurs at depths from 1 to 5μm. To collect as many electrons as possible, a p-n junction should be provided such that that distance the electrons have to diffuse to the junction is minimized. Thus, a p-n junction at around half this depth is optimal. Therefore, an N-Well is usually used to form the p-n junction since it occurs at around this depth.

[0018] A problem with this technique is that well implantation is not a critical parameter for CMOS transistors, and hence, is not particularly well controlled. The width of the collection node 14, shown by X in FIG. 1, varies from part-to-part and pixel-to-

pixel by a typical variation dX. The value of dX for the photodiode of FIG. 1 is typically ±300 nm. This variation in the width of the collection node 14 causes variation in the capacitance of the photodiode, leading to the abovementioned problem of mismatch between pixels.

[0019] FIG. 2 shows a modification that can be made to the structure of FIG. 1. Here, an N+ implant is used as the collection node. N+ is used to construct a transistor 26, and its implantation is very well controlled. The part-to-part and pixel-to-pixel variation, represented by dX2 in the photodiode of FIG. 2, typically has a value of ±100 nm.

[0020] Although this gives a photodiode with a more repeatable capacitance, its shallower depth means that its quantum efficiency is lower. For example, in FIG. 1, photo-generated electrons e1-e3 are most likely to be attracted to the well and be collected. In contrast, in FIG. 2, only electrons e2 will be sensed, with electrons e1 and e3 being lost into the well for the readout circuitry.

[0021] FIG. 3 shows a first embodiment of the present invention, which provides a deep yet accurate implant. Advanced CMOS technologies use a technique called shallow trench isolation (STI) to control accurately the width of (active) N+ or P+ areas. Photoresist is patterned outside the active areas. Anisotropic etching is used to etch a deep (typically 2 μm) trench. This provides a well defined edge for the implants. After implanting, polysilicon is deposited inside the trenches.

[0022] The present invention provides STI 30 around the collection node 28 to provide better control of the

width X of the collection node 28. As illustrated in FIG. 3, the N-well collection node 28 and the surrounding P-wells 16 have a depth of 3 μm below the upper surface of the epitaxial layer 10, and the STI has a depth of 2 μm.

[0023] In a method of manufacturing the photodiode, the STI is formed prior to implantation of the N-well, thus providing a definite border for the p-n junction to increase control of collection node 28 width X, with a typical value for dX3 being ±50 nm. This technique combines the advantage of a deep N-well for better quantum efficiency with better control of implantation, and hence capacitance. As dX3 << dX1, much better matching is obtained than N-Well implant photodiodes.

[0024] Ideally, the STI would be as deep, or deeper than the N-Well, as the p-n junction below the STI is a diffuse barrier. However, STI is usually formed at a depth of 2 μm. This is all that is required for transistors. In this situation, two thirds of the diode's capacitance is controlled accurately, which represents an improvement over the prior art. In addition, it is more economical to remain within the standard process flow, rather than producing a new technology having such an implant.

[0025] FIG. 4 illustrates a second embodiment of the present invention, which is applicable for relatively large photodiodes, having widths equal to or greater than 10 μm. Typically, large photodiodes will have widths between 40 and 60 μm. An N-well collection node 32 is bounded by STI 34. To increase sensitivity, the P-well 16 that is shown in FIGS. 1-3 is replaced by P-Epi. This means that all the electrons e1-e4 will most likely be collected by the collection node 32.

[0026] The structure of FIG. 4 provides a good approach for photodiodes, but design rule manuals prohibit this implementation for transistor design.

[0027] FIG. 5 shows a photodiode according to a third embodiment of the present invention. The critical n-p junction is at the N-Well/STI interface and is well controlled. However, the STI 34 of FIG. 4 is extended, so that the STI 38 of FIG. 5 extends over most of the pixel, suppressing P+ and hence avoiding DRC issues. This structure obtains good matching, but at the expense in a slight (5%) drop in quantum efficiency.

[0028] Variations and modifications can be made to the above without departing from the scope of the present invention. In particular, it will be apparent that the conductivity types of the various materials discussed could be reversed. For example, a P-well could be formed in an N-substrate rather than having an N-well formed in a P-substrate.